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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/084,803 | 02/28/2002 | Charles Douglas Murphy | | 7868 |

30320 7590 08/15/2005

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| EXAMINER | |
|---|---|
| JEANGLAUDE, JEAN BRUNER | |
| ART UNIT | PAPER NUMBER |
| 2819 | |

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/084,803 | MURPHY, CHARLES DOUGLAS | |
| | Examiner | Art Unit | |
| | Jean B. Jeanglaude | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *amedment filed on 12-15-03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-34* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## Response to Amendments/Arguments

1. The indicated allowability of claims 1 – 3, 5 – 34 is withdrawn in view of the newly discovered reference(s) to Hotta et al. (US Patent Number 4,381,495). Rejections based on the newly cited reference(s) follow.

2. The prosecution on this case is reopened.

## Drawing Objection

It is suggested to indicate the direction of the path of the signal in the drawings.

## *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 2, 12 - 18 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "first analog reference source comprises a first current source charging a first capacitor, whereby said means for causing said first analog reference signal to change as a function of time is said first current source and whereby said first analog reference signal is a voltage across said first capacitor" as recited in claim 2, does not reasonably provide enablement for "first analog reference source comprises a first current source charging a first capacitor, whereby said means for causing said first analog reference signal to change as a function of time is said first current source and whereby said first analog reference signal is a voltage across said first capacitor". The specification does not enable any person skilled in the art to which

it pertains, or with which it is most nearly connected, to –make --, -- use—, or – make and use -- the invention commensurate in scope with these claims. It is not seen in the drawings where these limitations are shown.

5. Also it is unclear where in the drawing where the "parallel DAC is implemented with a first counter and the first analog reference signal both being shared" as claimed by the applicant in claims 12, 17.

6. Claim 18 is automatically rejected due to the fact that it depends on claim 17 which is rejected under 112, 1st.

7. Claims 13 – 16 automatically rejected due to the fact that it depends on claim 12 which is rejected under 112, 1st

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 3, 4 – 7, 9 – 11, 17 – 29, 31 – 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Hotta et al. (US Patent Number 4,381,495).

10. Regarding claim 1, Hotta et al. discloses a machine used for digital-to-analog conversion (fig. 1) comprising : a first counter (6) which provides a first count; a first analog reference source (8) which provides a first analog reference signal; a first digital number value (UB) to be converted to a first analog value (fig. 1); means (clock generator 9) for causing the first count to change as a function of time (the clock is in

function of time); means for causing the first analog reference signal to change as a function of time (fig. 1); means (2) for detecting when the d first count reaches the first digital number value (the comparator compares the digital value with a reference number; col. 3, lines 50 - 56); means for recording the value of the first analog reference signal as the first analog value when the first count reaches the first digital number value whereby the first analog value is the converted value of said first digital number value (col. 4, lines 19 – 27; abstract).

11. Regarding claim 3, Hotta et al. discloses a machine (fig. 1) the means (9) for causing the first count to change as a function of time is a first digital clock (9).

12. Regarding clam 4, Hotta et al. discloses a machine (fig. 1) in which the first digital clock (9) has a frequency that can vary, whereby the first count need not always change at a single rate wherein high precision DAC is possible with a high frequency of the first digital clock a high rate of change of the first count and a corresponding high dynamic power consumption and low precision DAC is possible with a low frequency of the first digital clock, a low rate of change of the first count and a corresponding low dynamic power consumption (fig. 1).

13. Regarding claim 5, Hotta et al. discloses a machine (fig. 1) in which the first analog reference source (8) comprises a voltage ramp (fig. 1).

14. Regarding claim 6, Hotta et al. discloses a machine (fig. 1) in which the first analog reference source (9) comprises an operational amplifier (fig. 1).

15. Regarding claim 7, Hotta et al. discloses a machine (fig. 1) in which the first analog reference source comprises a first digital-to-analog converter (1) , whereby said

first count can be the input to the first digital-to-analog converter (fig. 1) and whereby the first analog reference signal (note the output of the DAC) can be the output of the first digital-to-analog converter (fig. 1).

16. Regarding claim 9, Hotta et al. discloses a machine (fig. 1) wherein the means (11) for recording the value of the first analog reference signal as the first analog value is a first sample-and-hold circuit (11, fig. 1).

17. Regarding claim 10, Hotta et al. discloses a machine (fig. 1) in which the first count controls the first analog reference source, whereby said first count need not be in increasing order or in decreasing order (fig. 1).

18. Regarding claim 11, Hotta et al. discloses a machine (fig. 1) in which the first count does not control the first analog reference signal, whereby the first count should be in increasing order or in decreasing order with said first analog reference signal level changing corresponding (fig. 1).

19. Regarding claim 19, Hotta et al. discloses a machine (fig. 1) further including means (9) for causing the first digital number value to change as a function of time, whereby the first analog value is the converted value of the first digital number value prior to its change with time, and represents the time required for the difference between the time-varying first count and the time-varying first digital number value to reach zero (fig. 1).

20. Regarding claim 20, Hotta et al. discloses a machine used for digital-to-analog conversion (fig. 1) comprising: a first counter (6) which provides a first count; means (the switch) for initializing the first count to a first digital number value (fig. 1); a first

analog reference source (8) which provides a first analog reference signal (fig. 1); means (9) for causing said first count to change as a function of time (fig. 1); means (9) for causing said first analog reference signal to change as a function of time (fig. 1); means [comparator](2) for detecting when the first count reaches a first digital threshold value (the comparator compares the digital value with a reference number; col. 3, lines 50 - 56); means for recording the value of the first analog reference signal as the first analog value when the first count reaches the first digital threshold value whereby the first analog value is the converted value of the first digital number value (col. 4, lines 19 – 27; abstract).

21. Regarding claim 21, Hotta et al. discloses a machine (fig. 1) further including: a second counter (4), which provides a second count; . means for initializing the second count to a second digital number value (fig. 1); means (9) for causing said second count to change as a function of time (fig. 1); means (2) for detecting when the second count reaches a second digital threshold value (fig. 1); means for recording the value of the first analog reference signal as the second analog value when the second count reaches the second digital threshold value whereby the first analog value is the converted value of the first digital number value and whereby the second analog value is the converted value of the second digital number value (col. 4, lines 19 – 27; abstract).

22. Regarding claim 22, Hotta et al. discloses a machine (fig. 1), which the first digital threshold value is the same as the second digital threshold value (fig. 1).

23. Regarding claim 23, Hotta et al. discloses a machine (fig. 1) in which the first digital threshold value is equal to zero (col. 4, lines 33 – 35).

24. Regarding claim 24, Hotta et al. discloses a machine (fig. 1) further including: a second counter (4) which provides a second count (fig. 1); second analog reference source (the input of the sampling circuit) which provides a second analog reference signal (fig. 1); means for initializing the second count to a second digital number value (fig. 1). Means (9) for causing the second count to change as a function of time (fig. 1); means for causing the second analog reference signal to change as a function of time (the clocking in the circuitry causes the analog reference to change in function of time);. Means (2) for detecting when the second count reaches a second digital threshold value (fig. 1); means for recording the value of the second analog reference signal as the second analog value when the second count reaches the second digital threshold value whereby said first analog value is the converted value of the first digital number value and whereby the second analog value is the converted value of the second digital number value (col. 4, lines 19 – 27; abstract)[the sample and hold is used to record the value of the analog reference signal].

25. Regarding claim 25, Hotta et al. discloses a machine (fig. 1) in which the first digital threshold value is the same as said second digital threshold value (fig. 1).

26. Regarding claim 26, Hotta et al. discloses a machine (fig. 1) in which the first digital threshold value is equal to zero (col. 4, lines 33 – 35).

27. Regarding claim 27, Hotta et al. discloses a digital-to-analog converter (fig. 1) comprising a first circuit element (6) wherein the first circuit element (6) is used in a

first instance for a first conversion of a first digital number to a first analog value (fig. 1) the first circuit element (6) is also used in the first instance for a second conversion of a second digital number to a second analog value (fig. 1)[note a the input of the DAC 1 there are the UB and LB that are used at different time in the process to produce an analog signal at the output of the DAC 1]; the first circuit element (6) comprises a first parameter (the clock 9) that varies with time during a conversion operation whereby the first circuit element is effectively shared in the first conversion and in the second conversion, rather than used in said first instance for said first conversion and separately in a second instance for said second conversion, and whereby the first circuit element is not simply a constant reference signal. (fig. 1).

28. Regarding claim 28, Hotta et al. discloses a digital-to-analog converter (fig. 1in which the first circuit element (6) is a first counter (6, fig. 1)

29. Regarding claim 29, Hotta et al. discloses a digital-to-analog converter (fig. 1) further including: a first digital comparator (2) providing a first digital comparator output (fig. 1) . means for averaging said the digital comparator output over time whereby the digital-to-analog converter (1) can implement shared parallel pulse-width modulation digital-to-analog conversion (figs. 2, 4).

30. Regarding claim 31, Hotta et al. discloses a digital-to-analog converter (fig. 1) in which the first circuit element (6) is a first analog reference source (fig. 1).

31. Regarding claim 32, Hotta et al. discloses a machine used for digital-to-analog conversion (fig. 1) , comprising: a first counter (6) which provides a first count (fig 1) . means for initializing said first count to a first digital number value (fig. 1); means (9) for

causing the first count to change as a function of time (fig. 1);. means (2) for detecting when the first count reaches a first digital threshold value (fig. 1); means for averaging the output of the means for detecting when the first count reaches a first digital threshold whereby the output of the means for averaging is the converted value of said first digital number value (fig. 1).

32. Regarding claim 33, Hotta et al. discloses a machine (fig. 1) means (2) for detecting when the first count reaches a first digital threshold value is a first digital comparator (fig. 1).

33. Regarding claim 34, Hotta et al. discloses a machine (fig. 1) in which said first digital threshold level is zero, whereby no storage means are necessary to hold the value of the first digital threshold level and whereby the means (2) for detecting when the first count reaches the first digital threshold level can be implemented with simple digital logic such as a single multiple-input AND gate (30) [fig. 1].

***Claim Rejections - 35 USC § 103***

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hotta et al. in view of Sakuragi (US Patent Number 6,542,105).

36. Regarding claim 30, Hotta et al. does not specifically disclose an analog-to-digital converter comprising the digital-to-analog converter, whereby parallel analog-to-digital

conversion of a multiplicity of analog values to a multiplicity of digital number values can share said first circuit element. However, Sakuragi, in a related field, discloses an ADC (fig. 1) that implements a DAC (2) whereby parallel analog-to-digital conversion of a multiplicity of analog values to a multiplicity of digital number values can share a circuit element (counter) [1] (fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hotta et al.'s system with that of Sakuragi in order to enhance an ADC speed while maintaining the ADC conversion.

**Allowable Subject Matter**

37. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

38. Reasons for allowing this claim will be provided in the next office action.

39. Claims 2, 12 – 18 will be objected as claims having allowable subject matter upon complying to the 112, 1st rejection above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callaham can be reached on 571-272-1740. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
August 12, 2005